Notice of Allowability	Application No.	Applicant(s)	
	10/674,869	YIN ET AL.	
	Examiner	Art Unit	
	Khanh Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the preliminary amendment filed August 13, 2004*.

2. ☒ The allowed claim(s) is/are *48-78*.

3. ☒ The drawings filed on *29 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *09/943,897* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/29/03 & 8/13/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

Response to Amendment

This Office Action is in response to the Preliminary Amendment filed on August 13, 2004.

Accordingly, claims 48-51 were amended, claims 1-47 were canceled, and new claims 52-78 were added.

Currently, claims 48-78 are pending in the application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/943,897 filed on August 30, 2001.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on September 29, 2003 and August 13, 2004 are being considered by the examiner.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Edward S. Hotchkiss on October 1, 2004.

The application has been amended as follows:

In the Title:

Please amend the Title as follows: --METHOD OF MANUFACTURING WIRE BONDED MICROELECTRONIC DEVICE ASSEMBLIES--.

In the Claims:

In claim 48: line 15, after "positioning the", delete "microelectronic component" and substitute therein with --semiconductor die--; and line 16, after "surface of the", delete "microelectronic component" and substitute therein with --semiconductor die--.

In claim 78: line 11, before "first surface", delete "the" and substitute therein with --a--.

Allowable Subject Matter

Claims 48-78 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record, taken alone or in combination, discloses all the features as claimed.

Re claim 48, none of the prior art of record discloses a process of electrically coupling a semiconductor die having an integrated circuit to a substrate, comprising: forming a multi-layer bond pad by: depositing an intermediate bond layer of a first metal on an outer surface of an integrated bond pad carried by a first surface of the semiconductor die, the integrated bond pad and the integrated circuit being formed of a second metal selected from the group consisting of aluminum and copper; and thereafter, depositing an outer bond layer on the intermediate bond layer, the outer bond layer comprising a third metal, which is different from the first metal and the second metal; positioning the semiconductor die with respect to the substrate with the first surface of the semiconductor die spaced from a contact surface of the substrate; ball bonding a first end of a bonding wire to a contact carried by the contact surface of the substrate, the

bonding wire comprising the third metal; and stitch bonding a second end of the bonding wire to the outer bond layer of the multi-layer bond pad.

Re claim 59, none of the prior art of record discloses a process of electrically coupling a microelectronic component to a substrate, comprising: forming a multi-layer bond pad by: depositing a passivation layer on a first surface of the microelectronic component, the first surface carrying an integrated bond pad that has a surface area and is formed of a first metal, wherein an effective surface area of the integrated bond pad, which is less than the surface area of the integrated bond pad, is exposed by an opening of the passivation layer; depositing an intermediate bond layer of a second metal on the effective surface area of the integrated bond pad; and depositing an outer bond layer on the intermediate bond layer, the outer bond layer comprising a third metal that differs from the first metal; positioning the microelectronic component with respect to the substrate with the first surface of the microelectronic component spaced from a contact surface of the substrate; ball bonding a first end of a bonding wire to a contact carried by the contact surface of the substrate, the bonding wire comprising the third metal; and stitch bonding a second end of the bonding wire to the outer bond layer of the multi-layer bond pad.

Re claim 71, none of the prior art of record discloses a process of electrically coupling a microelectronic component to a substrate, comprising: forming first and second multi-layer bond pads by: depositing an intermediate bond layer of a first metal on a first surface of a microelectronic component, the first surface carrying first and second bond pads that each comprise a second metal; depositing a process layer having a first opening associated with the first bond pad and a second opening associated with the second bond pad; depositing an outer

bond layer of a third metal on the intermediate bond layer in each of the first and second openings; and removing the process layer; attaching the microelectronic component to the substrate with the first surface of the microelectronic component spaced from a contact surface of the substrate; ball bonding a first end of a bonding wire to a contact carried by the contact surface of a substrate, the bonding wire comprising the third metal; and stitch bonding a second end of the bonding wire to the outer bond layer of the first multi-layer bond pad.

Re claim 78, none of the prior art of record discloses a process of electrically coupling a microelectronic component to a substrate, the microelectronic component having an integrated circuit and an integrated bond pad, both of which comprise a first metal selected from a group consisting of copper and aluminum, the process comprising: forming a multi-layer bond pad by: depositing an intermediate bond layer of a second metal on an outer surface of the integrated bond pad, the second metal being selected from a group consisting of titanium, tungsten, and chromium; and depositing an outer bond layer comprising gold on the intermediate bond layer; attaching the microelectronic component to the substrate with the first surface of the microelectronic component spaced from a contact surface of the substrate; ball bonding a first end of a bonding wire to a contact carried by the contact surface of the substrate, the bonding wire comprising gold; and stitch bonding a second end of the bonding wire to the outer bond layer of the multi-layer bond pad.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Thursday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

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